Ordering number : EN6037

CMOS IC

LC72723, LC72723M

RDS Demodulation IC

Overview

The LC72723 is an RDS (Radio Data System) signal demodulation IC. This IC integrates a bandpass filter, the demodulation circuit, and buffer RAM on a single chip and can read out RDS data in slave mode operation with the provision of an external clock input. It also supports master mode, in which the data is read out in synchronization with an RDS clock output provided by the IC itself.

Functions

- Bandpass filter: Switched capacitor filter (SCF)
- RDS demodulation: Functions include 57kHz carrier regeneration, clock regeneration, biphase decoding, and differential decoding
- Buffer RAM: Stores 128 bits (about 100 ms) of data.
- Data output: Output can be switched between master mode and slave mode readout.
- RDS ID detection: Supports ID reset
- Standby control: Stops the crystal oscillator.
- Fully adjustment free.

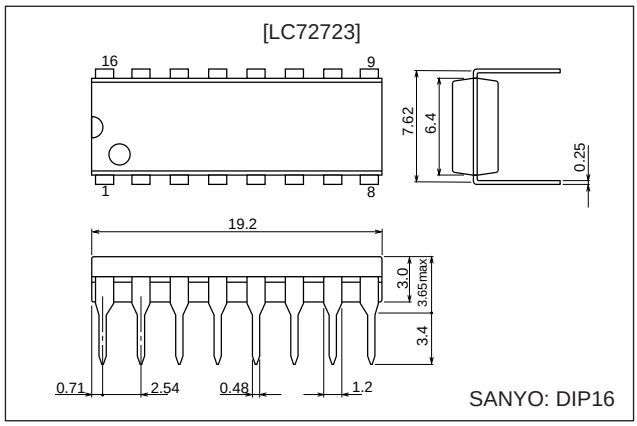
Ratings

- Operating supply voltage: 4.5 to 5.5 V
- Operating temperature: –40 to 85°C
- Packages: DIP16 and MFP16

Package Dimensions

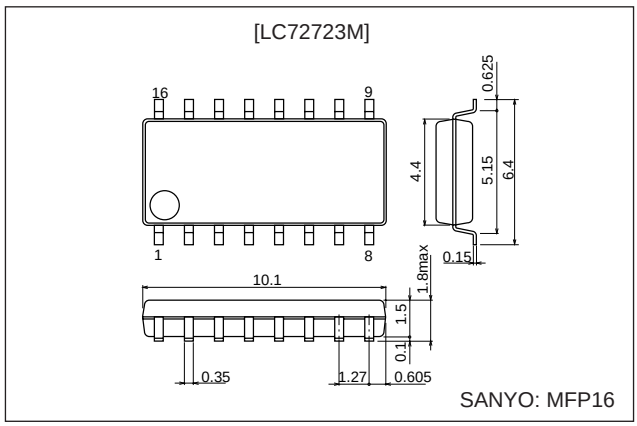
unit: mm

3006B-DIP16



unit: mm

3035A-MFP16



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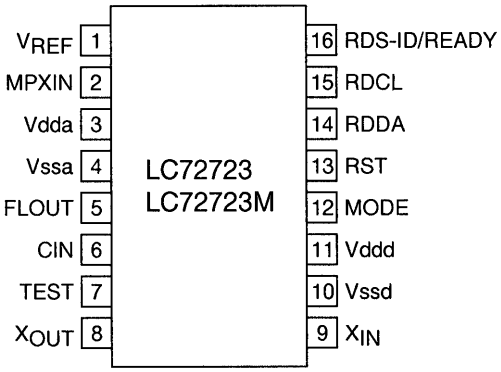
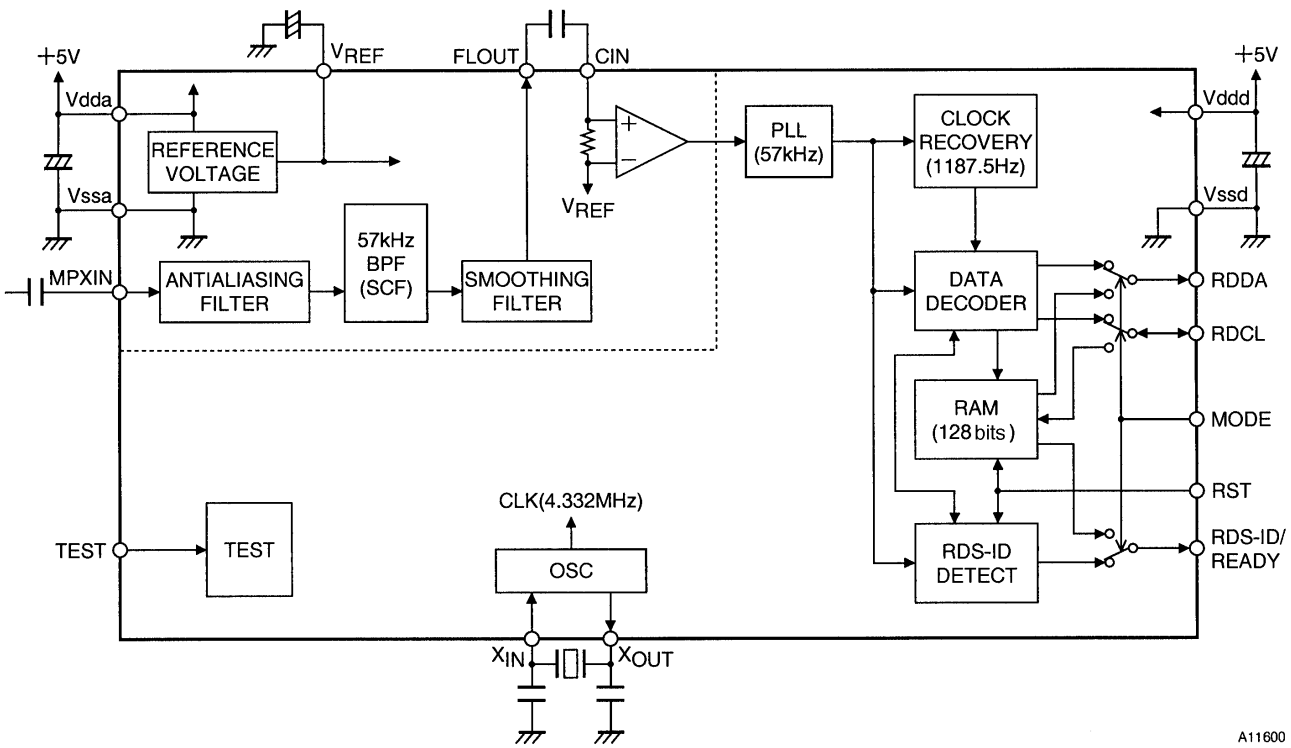
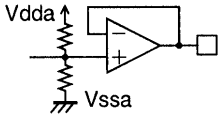
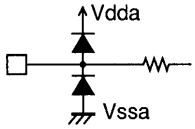
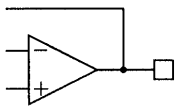
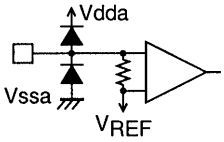
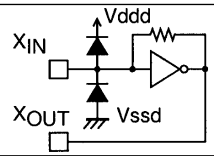
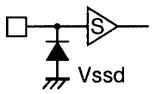
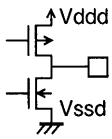
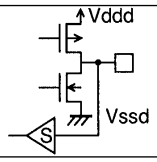
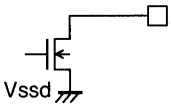
Pin Assignment (DIP16/MFP16)



Block Diagram



Pin Descriptions

Pin No.	Pin	Function	I/O	Pin circuit type
1	VREF	Reference voltage output (Vdda/2)	Output	
2	MPXIN	Base band (multiplex) signal input	Input	
5	FLOUT	Subcarrier output (filter output)	Output	
6	CIN	Subcarrier input (comparator input)	Input	
3	Vdda	Analog system power supply (+5 V)	—	—
4	Vssa	Analog system ground	—	—
8	XOUT	Crystal element output (4.332 MHz)	Output	
9	XIN	Crystal element input (or external reference signal input)	Input	
7	TEST	Test input		
12	MODE	Readout mode setting (0: master, 1: slave)		
13	RST	RDS ID and RAM reset (Active high logic)		
14	RDDA	RDS data output	Output	
15	RDCL	RDS clock output (master mode) RDS clock input (slave mode)	I/O	
16	RDS-ID/READY	RDS ID/ready output (Active low)	Output	
11	Vddd	Digital system power supply (+5 V)	—	—
10	Vssd	Digital system ground	—	—

Specifications

Absolute Maximum Ratings at Ta = 25°C, Vssd = Vssa = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Vddd, Vdda *	–0.3 to 7.0	V
Maximum input voltage	$V_{IN}1$ max	TEST, MODE, RST	–0.3 to +7.0	V
	$V_{IN}2$ max	XIN, RDCL	–0.3 to Vddd + 0.3	V
	$V_{IN}3$ max	MPXIN, CIN	–0.3 to Vdda + 0.3	V
Maximum output voltage	Vo1 max	RDS-ID (READY)	–0.3 to +7.0	V
	Vo2 max	XOUT, RDDA, RDCL	–0.3 to Vddd + 0.3	V
	Vo3 max	FLOUT	–0.3 to Vdda + 0.3	V
Maximum output current	Io1 max	XOUT, FLOUT, RDDA, RDCL	+3.0	mA
	Io2 max	RDS–ID (READY)	+20.0	mA
Allowable power dissipation	Pd max	(Ta ≤ 85°C)	DIP16 : 300	mW
			MFP16 : 140	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

*: Note that Vdda must be less than or equal to Vddd + 0.3 V

Allowable Operating Ranges at Ta = –40 to +85°C, Vssd = Vssa = 0 V, Vddd = Vdda

Parameter	Symbol	Conditions		Ratings			Unit
				min	typ	max	
Supply voltage	V_{DD}	Vddd, Vdda: Vddd = Vdda		4.5	5.0	5.5	V
High-level input voltage	$V_{IH}1$	TEST, MODE, RST		07 Vddd		6.5	V
	$V_{IH}2$	RDCL		0.7 Vddd		Vddd	V
Low-level input voltage	V_{IL}	TEST, MODE, RST, RDCL		0		0.3 Vddd	V
Output voltage	Vo1	RDDA, RDCL				Vddd	V
	Vo2	RDS–ID (READY)				6.5	V
Input amplitude	$V_{IN}1$	MPXIN	f = 57 ±2 KHz			50	mVrms
	$V_{IN}2$		100% modulation, composite	100			mVrms
	VX_{IN}	XIN		400		1500	mVrms
Guaranteed oscillator operating range	Xtal	XIN, XOUT: C1 ≤ 120 Ω			4.332		MHz
Crystal oscillator frequency deviation	TXtal	XIN, XOUT: Fo = 4.332 MHz				±100	ppm
RDCL setup time	t_{CS}	RDCL, RDDA		0			µs
RDCL high-level time	t_{CH}	RDCL		0.75			µs
RDCL low-level time	t_{CL}	RDCL		0.75			µs
Data output time	t_{DC}	RDCL, RDDA				0.75	µS
READY output time	t_{RC}	RDCL, READY				0.75	µs
READY low-level time	t_{RL}	READY				107	ms

Electrical Characteristics at Ta = –40 to +85°C, Vssd = Vssa = 0 V, Vddd = Vdda

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input resistance	Rmpxin	MPXIN-Vssa: f = 57 KHz		23		KΩ
	Rcin	CIN-Vssa: f = 57 KHz		100		KΩ
Internal feedback resistance	Rf	XIN		1.0		MΩ
Center frequency	fc	FLOUT	56.5	57.0	57.5	KHz
–3dB bandwidth	BW–3dB	FLOUT	2.5	3.0	3.5	KHz
Gain	Gain	MPXIN-FLOUT: f = 57 KHz	28	31	34	dB
Stop band attenuation	Att1	FLOUT: $\Delta f = \pm 7$ KHz	30			dB
	Att2	FLOUT: f < 45 KHz, f > 70 KHz	40			dB
	Att3	FLOUT: f < 20 KHz	50			dB
Reference voltage output	Vref	Vref: Vdda = 5 V		2.5		V
Hysteresis	V_{HIS}	TEST, MODE, RST, RDCL		0.1 Vddd		V
Low-level output voltage	V_{OL1}	RDDA, RDCL : I = 2 mA			0.4	V
	V_{OL2}	RDS-ID (READY): I = 8 mA			0.4	V
High-level output voltage	V_{OH}	RDDA, RDCL : I = 2 mA	Vddd – 0.4			V
High-level input current	$I_{IH}1$	TEST, MODE, RST, RDCL : V_I = 6.5 V			5.0	µA
	$I_{IH}2$	XIN: V_I = Vddd	2.0		11	µA
Low-level input current	$I_{IL}1$	TEST, MODE, RST, RDCL : V_I = 0 V			5.0	µA
	$I_{IL}2$	XIN: V_I = 0 V	2.0		11	µA
Output off leakage current	I_{OFF}	RDS-ID (READY): V_O = 6.5 V			5.0	µA
Current drain	Idd	Vddd + Vdda		8		mA

Inputs and Outputs

TEST	MODE	Circuit operating mode	RDCL pin	RDS-ID/READY pin
0	0	Master mode	Clock output	RDS-ID output
0	1	Slave mode	Clock input	READY output
1	0	Standby mode (crystal oscillator stopped)	—	—
1	1	IC test mode (Cannot be set by users.)	—	—

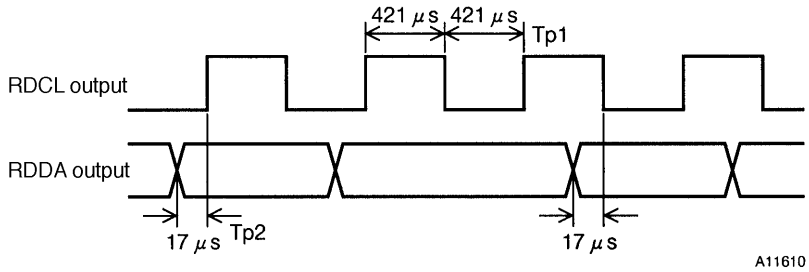
	RST pin
RST = 0	Normal operation
RST = 1	The RDS-ID and demodulation circuits are cleared, and (in slave mode) the READY state and memory are cleared.

	RDS ID/READY pin
Master mode	RDS-ID output (active low)
Slave mode	Readout data ready output (active low)

Note: The RDS-ID (READY) pin is an n-channel open-drain output, and data is read out by connecting a pull-up resistor.

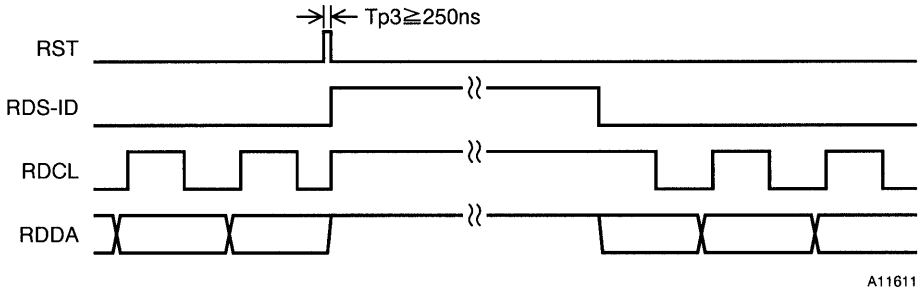
RDCL/RDDA Output Timing

• Master mode



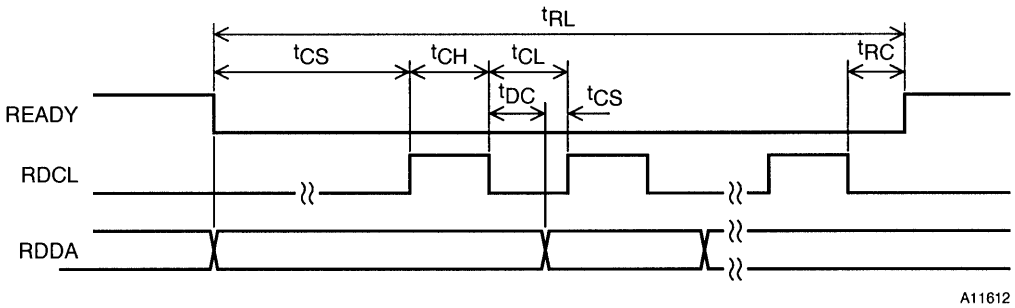
RST Operation

• Master mode



Caution: After an RST input, the RDCL and RDDA outputs stop at the high level until the first RDS ID detection.

RDCL Control in Slave Mode

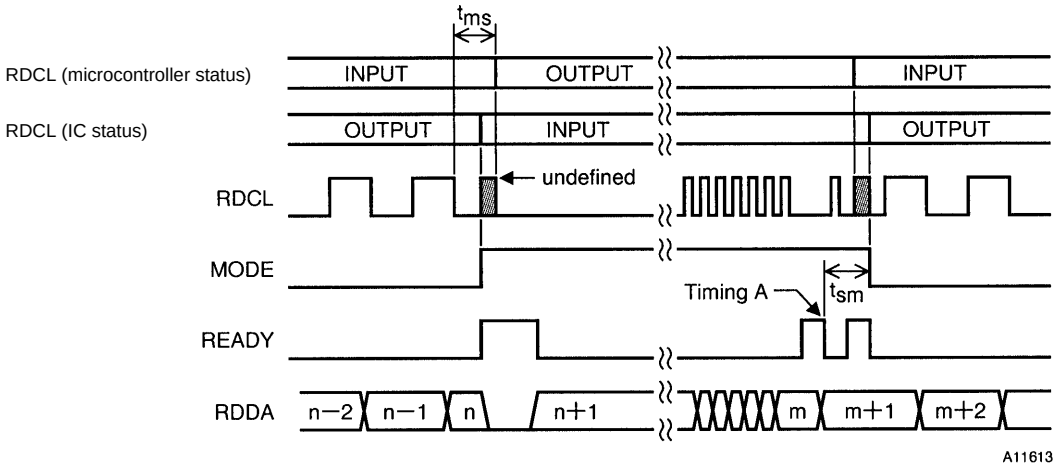


Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
RDCL setup time	t_{CS}	RDCL, RDDA	0			μs
RDCL high-level time	t_{CH}	RDCL	0.75			μs
RDCL low-level time	t_{CL}	RDCL	0.75			μs
Data output time	t_{DC}	RDCL, RDDA			0.75	μs
READY output time	t_{RC}	RDCL, READY			0.75	μs
Ready low-level time	t_{RL}	READY			107	ms

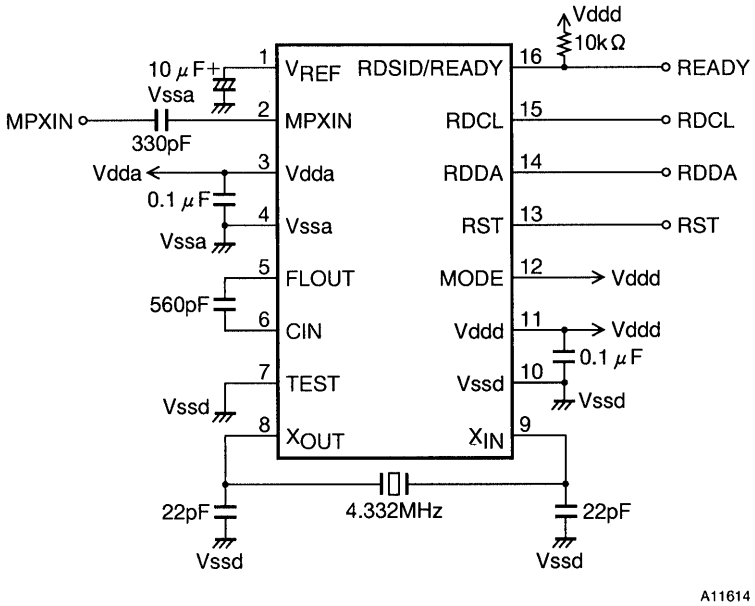
Notes:1. Start RDCL clock input after the READY signal goes low. Applications must stand by with RDCL held low when the READY pin is high.
2. Each time the RDCL input is switched from low to high to low, the application must check the READY signal level after the period t_{RC} has elapsed once RDCL has been set low. If READY is at the low level, the application may apply the next RDCL clock cycle. If READY is high, the application must stop RDCL input at that point.
3. When the above timing conditions are met, RDDA can be read at either the rise or fall of the RDCL signal.
4. After the last data from memory has been read, READY will be high once the period t_{RC} has elapsed after the fall of the RDCL signal. If even 1 bit of data has been written to memory, READY will be low and the application will be able to read that data.

5. When switching channels, it is desirable to immediately reset memory and the READY pin with an RST input. If this is not done, data received on the previous channel may remain in memory. When the IC is reset, data is not written until the RDS-ID is detected, and therefore, the READY signal will go low after the RDS-ID is detected. (Although the RDS-ID is not output in slave mode, it is detected internally in the IC.) After an RST input, once an RDS-ID has been detected, all received data will be written to memory regardless of the RDS-ID detection state.

6. The readout mode may be switched between master and slave modes during readout. Applications must observe the following points to assure data continuity during this operation.
   - Data acquisition timing in master mode
     Data must be read on the falling edge of RDCL.
   - Timing of the switch from master mode to slave mode
     After the RDCL output goes low and the RDDA data has been acquired, the application must set MODE high immediately. Then, the microcontroller starts output by setting the RDCL signal low. The microcontroller RDCL output must start within 840 µs (tms) after RDCL went low. In this case, if the last data read in master mode was data item n, then data starting with item n+1 will be written to memory.
   - Timing of the switch from slave mode to master mode
     After all data has been read from memory and READY has gone high, the application must then wait until READY goes low once again the next time (timing A in the figure), immediately read out one bit of data and input the RDCL clock. Then, at the point READY goes high, the microcontroller must terminate RDCL output and then set MODE low. The application must switch MODE to low within 840 µs (tms) after READY goes low (timing A in the figure).



LC72723 Sample Application Connection Circuit (for slave mode operation)



Caution: If the RST pin is unused, it must be connected to ground.

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